Sirindhorn International Institute of Technology

Thammasat University at Rangsit

School of Information, Computer and Communication Technology

ECS 371: Problem Set 9

Due date: September 16, 2009 (Wednesday)

Instructions

1. Only ONE of the problems will be graded. Of course, you do not know which problems will be selected; so you should work on all of them.
2. Late submission will not be accepted.
3. **Write down all the steps** that you have done to obtain your answers. You may not get full credit even when your answer is correct without showing how you get your answer.

Part A

Your scores WILL be substantially reduced if no explanation is provided.
You scores may exceed the full score when excellent explanation is provided.

Use the design technique presented in lecture 21 and 22 to solve the following problems.

1. Design a state machine which simultaneously satisfies all of the following requirements:

   a) Have one-bit input signal called W.
   b) Have one-bit output signal called Y.
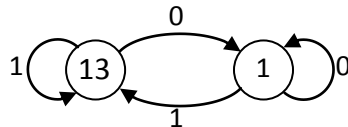   c) The counting sequence agrees with the following state diagram:
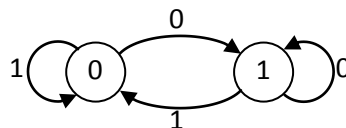
   The numbers on the arrows indicate the values of W.

d) Use exactly one D flip-flop.

e) Additional AND, OR, NOT gates are allowed.

2. Design a state machine which simultaneously satisfies all of the following requirements:

a) Have one-bit input signal called W.

b) Have four-bit output signals called Y_3 Y_2 Y_1 and Y_0.
   Y_3 is the MSB.

c) The counting sequence agrees with the following state diagram:

The numbers on the arrows indicate the values of W.

d) The output is simply the unsigned binary representation of the state in the state transition diagram.

e) Use exactly one D flip-flop.

f) Additional AND, OR, NOT gates are allowed.

3. Design a counter which simultaneously satisfies all of the following requirements:

a) Have no input signal.

b) Have two-bit output signals called Y_1 and Y_0.
   Y_1 is the MSB.

c) The counting sequence agrees with the following state diagram:
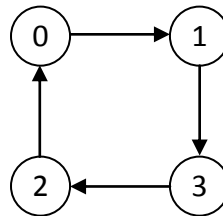
d) Use exactly one D flip-flop and one J-K flip-flop.

e) The counter output Y_0 is the output of the J-K flip-flop.

f) The counter output Y_1 is the output of the D flip-flop.

g) No additional gate allowed.

Part B:

- No question is assigned for this part.