# Sirindhorn International Institute of Technology Thammasat University at Rangsit 

School of Information, Computer and Communication Technology

## ECS 371: Problem Set 8

Semester/Year: 1/2009
Course Title: Digital Circuits
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Course Web Site: http://www.siit.tu.ac.th/prapun/ecs371/

Due date: September 9, 2009 (Wednesday)

## Instructions

1. The questions in part $B$ are assigned from the following textbook:

Thomas L. Floyd, Digital Fundamentals, $10^{\text {th }}$ Edition, Pearson Education International (2009).
2. Only ONE of the problems will be graded. Of course, you do not know which problems will be selected; so you should work on all of them.
3. Late submission will not be accepted.
4. Write down all the steps that you have done to obtain your answers. You may not get full credit even when your answer is correct without showing how you get your answer.

## Part A

Your scores WILL be substantially reduced if no explanation is provided.
You scores may exceed the full score when excellent explanation is provided.
Use the design technique presented in lecture 21 and 22 to solve the following problems.

1. Construct a D flip-flop from a J-K flip-flop. You may use additional AND, OR, NOT gates.
2. Construct a counter whose counting sequence satisfies the state transition diagram below. Use D FFs.

3. Find the "complete" state transition diagram (which includes all states) for the counter you constructed in problem 2.
4. Draw the waveforms of the outputs from the counter you constructed in problem 2. Assume " 2 " is the initial state. Provide at least 6 clock periods.
5. Repeat problem 2 but use J-K FFs.
6. Construct the counter as in problem 2. There should be a count enable (CTEN) input as well.
7. Construct the counter as in problem 5. There should be a count enable (CTEN) input as well.

## Part B: Chapter 8

- Please submit your solutions for the following questions: 18

18. Design a counter to produce the following sequence. Use J-K flip-flops.
$00,10,01,11,00, \ldots$
