

Sirindhorn International Institute of Technology
Thammasat University at Rangsit
School of Information, Computer and Communication Technology

ECS 371: Problem Set 7

Semester/Year: 1/2009

Course Title: Digital Circuits

Instructor: Dr. Prapun Suksompong (prapun@siit.tu.ac.th)

Course Web Site: <http://www.siiit.tu.ac.th/prapun/ecs371/>

Due date: August 26, 2009 (Wednesday)

Instructions

1. The questions in part B are assigned from the following textbook:

Thomas L. Floyd, [*Digital Fundamentals*](#), 10th Edition, Pearson Education International (2009).
2. Only ONE of the problems will be graded. Of course, you do not know which problems will be selected; so you should work on all of them.
3. Late submission will not be accepted.
4. **Write down all the steps** that you have done to obtain your answers. You may not get full credit even when your answer is correct without showing how you get your answer.

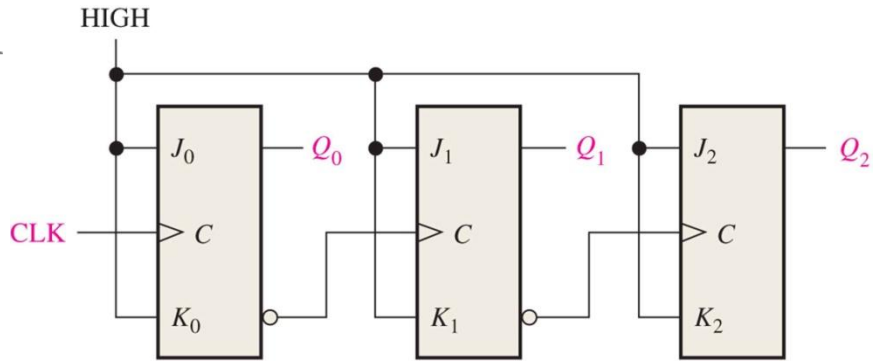
Part A

1. Construct a J-K flip-flop from a D flip-flop. You may use additional AND, OR, NOT gates.

Part B: Chapter 8

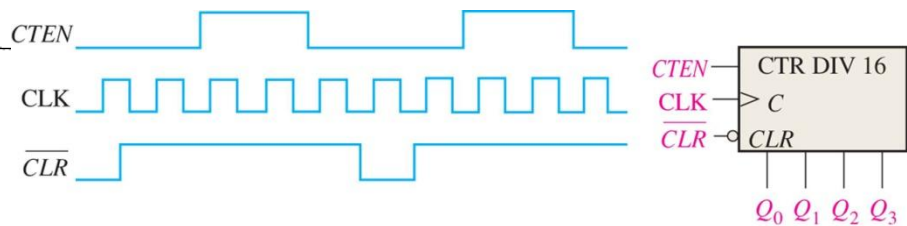
- Please submit your solutions for the following questions: **2, 4(b,d), 8, 10, 16**
2. For the ripple counter in Figure 8–70, show the complete timing diagram for sixteen clock pulses. Show the clock, Q_0 , Q_1 , and Q_2 waveforms.

▶ FIGURE 8-70



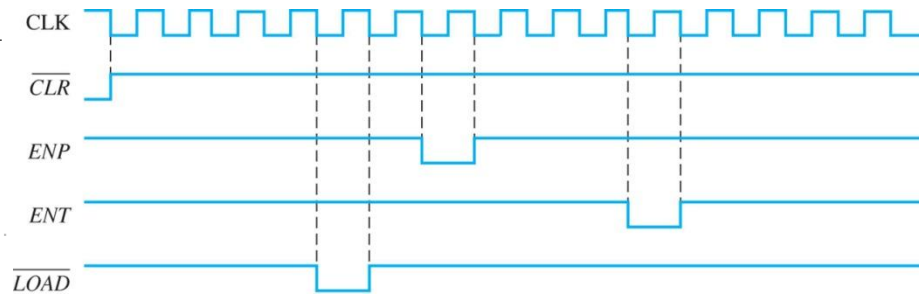
4. Show how to connect a 74LS93 4-bit asynchronous counter for each of the following moduli:
 (a) 9 (b) 11 (c) 13 (d) 14 (e) 15
8. The waveforms in Figure 8-73 are applied to the count enable, clear, and clock inputs as indicated. Show the counter output waveforms in proper relation to these inputs. The clear input is asynchronous.

▶ FIGURE 8-73



10. The waveforms in Figure 8-75 are applied to a 74HC163 binary counter. Determine the Q outputs and the RCO . The inputs are $D_0 = 1$, $D_1 = 1$, $D_2 = 0$, and $D_3 = 1$.

▶ FIGURE 8-75



16. Determine the sequence of the counter in Figure 8-77.

FIGURE 8-77

