

Sirindhorn International Institute of Technology  
Thammasat University at Rangsit  
School of Information, Computer and Communication Technology

## ECS 371: Problem Set 5

**Semester/Year:** 1/2009

**Course Title:** Digital Circuits

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**Course Web Site:** <http://www.siit.tu.ac.th/prapun/ecs371/>

**Due date:** Not due

1. In class, we implemented a full-adder using a 3:8 decoder and two OR gates. For this question, implement a full-adder using two 74x151s.

2. What are the full-adder inputs that will produce each of the following outputs:

(a)  $\Sigma = 0, C_{\text{out}} = 0$

(b)  $\Sigma = 1, C_{\text{out}} = 0$

(c)  $\Sigma = 1, C_{\text{out}} = 1$

(d)  $\Sigma = 0, C_{\text{out}} = 1$

3. Determine the outputs of a full-adder for each of the following inputs:

(a)  $A = 1, B = 0, C_{\text{in}} = 0$

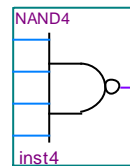
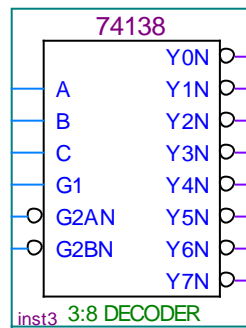
(b)  $A = 0, B = 0, C_{\text{in}} = 1$

(c)  $A = 0, B = 1, C_{\text{in}} = 1$

(d)  $A = 1, B = 1, C_{\text{in}} = 1$

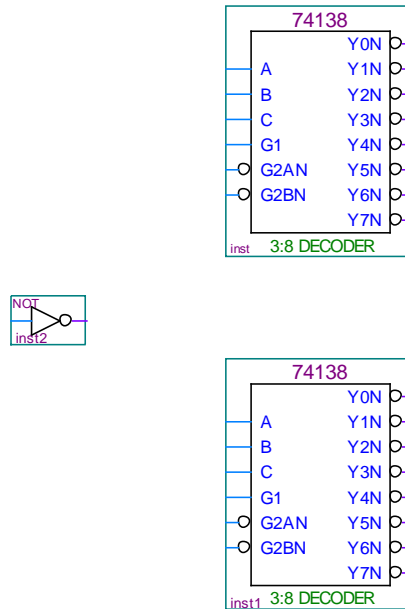
4. Implement the logic function specified in the table below by using only a 74x138 and a NAND gate.

Input			Output
X	Y	Z	W
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



Your score depends strongly on your explanation of your answer. Zero score may be given even for a correct answer if the explanation is incomplete.

5. Construct a 4:16 decoder with an active-HIGH enable (EN) and active-LOW outputs from two 74x138 decoders and one NOT gate. Label the inputs of the 4:16 decoder by  $I_3$   $I_2$   $I_1$   $I_0$  where  $I_3$  is the MSB. Label the outputs of the 4:16 decoder by  $O_{15}$   $O_{14}$   $O_{13}$   $O_{12}$  ...  $O_1$   $O_0$ .



Again, your score depends strongly on your explanation of your answer. Zero score may be given even for a correct answer if the explanation is incomplete.